CLAIMS

1.   An oscillator comprising:

        a first flip-flop; and

        a second flip-flop coupled with the first flip-flop to provide an oscillating

5   signal.

2.   An oscillator as recited in Claim 1, wherein the oscillating signal has an

oscillation frequency close to a maximum toggling frequency of the flip-flop.

3.   An oscillator as recited in Claim 1, wherein the first and the second flip-flops are

configured in a feedback arrangement.

10   4.   An oscillator as recited in Claim 1, wherein the first and the second flip-flops are

configured in a feedback arrangement wherein the oscillating signal is fed back to a first

clock input of the first flip-flop and a second clock input of the second flip-flop.

5.   An oscillator as recited in Claim 1, wherein the first and the second flip-flops are

configured in a cross-coupled feedback arrangement.

15   6.   An oscillator as recited in Claim 1, wherein:

        the first and the second flip-flops are configured in a cross-coupled

feedback arrangement wherein the oscillating signal is fed back to a first clock

input of the first flip-flop and a second clock input of the second flip-flop, and

        the oscillating signal has a positive transition and a negative transition and

20   clock inputs of the first and the second flip-flops are configured to trigger on

opposite transitions of the oscillating signal.

7.   An oscillator as recited in Claim 1, wherein the first and the second flip-flops are configured in a cross-coupled feedback arrangement to toggle alternately.

8.   An oscillator as recited in Claim 1, wherein the oscillating signal is applied to a circuit that includes a circuit flip-flop, and the first and second flip-flops are substantially the same type as the circuit flip-flop.

9.   An oscillator as recited in Claim 1, wherein the oscillating signal is applied to a circuit, and the oscillator resides on the same die as the circuit.

10.   An oscillator as recited in Claim 1, further comprising an interface for receiving a startup signal configure to start oscillation.

11.   An oscillator as recited in Claim 1, further comprising a clock buffer configured to buffer the oscillating signal.

12.   An oscillator as recited in Claim 1, wherein the oscillating signal is provided to a primary circuit via a primary circuit buffer and further comprising an oscillating signal buffer configured to buffer the oscillating signal in the same manner that the primary circuit buffer buffers the oscillating signal as provided to the primary circuit.

13.   An oscillator as recited in Claim 1, wherein the oscillating signal is sent to a field programmable gate array (FPGA).

14.   An oscillator as recited in Claim 1, wherein the oscillating signal is sent to an application specific integrated circuit (ASIC).

15.   An oscillator as recited in Claim 1, wherein the oscillating signal is monitored.

16.   An oscillator as recited in Claim 1, wherein the oscillating signal is monitored and the oscillator is restarted if it is determined that the output has ceased to oscillate.

17.   A method of generating an oscillating signal, comprising:

providing the oscillating signal as a first clock input to a first flip flop;

inverting the oscillating signal and providing the inverted oscillating

signal as a second clock input to a second flip flop;

using the output of the first flip flop and the output of the second flip flop

5   to generate a combined output that alternates between a logic low level and a

logic high level; and

using the combined output to sustain the oscillation of the oscillating

signal.

18.   The method of Claim 17 further comprising providing a startup signal to generate

10   a first pulse of the oscillating signal.

19.   The method of Claim 17 further comprising buffering the combined output and

providing the buffered combined output as the oscillating signal.

20.   An oscillator comprising:

a first element configured to toggle a first data output according to a first

15   transition of an oscillating signal;

a second element configured to toggle a second data output according to a

second transition of the oscillating signal;

a third element configured to receive the first data output and the second

data output as inputs and provide the oscillating signal as output.

20   21.   A method of generating an oscillating signal, comprising:

toggling a first data output according to a first transition of the oscillating

signal;

toggling a second data output according to a second transition of the oscillating signal;

using the first data output and the second data output to generate an alternating output that sustains the oscillation of the oscillating signal.

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